

What is claimed is:

1. A low power flip-flop circuit comprising:
 - a latch that receives and holds an input signal responsive to an internal clock signal;
 - 5 a comparing circuit that compares the input signal with an output signal of the latch to provide a comparison signal indicative thereof; and
 - an internal clock generating circuit that receives an external clock signal and generates the internal clock signal under control of the comparison signal, wherein the internal clock generating circuit controls passing of the
 - 10 external clock signal responsive to the comparison signal, delays the external clock signal for a predetermined time, inverts the delayed external clock signal, and generates the internal clock signal as having a pulse width smaller than a pulse width of the external clock signal by performing a NAND operation on the external clock signal and the inverted delayed external clock signal, the internal
 - 15 clock signal having rising and falling edges which are all synchronized with the external clock signal.
2. The low power flip-flop circuit according to claim 1, wherein the internal clock generating circuit comprises:
 - 20 an inverter that inverts the comparison signal as provided at a first node and transmits the inverted comparison signal to a second node;
 - a transmission gate, having a first input terminal connected to the first node and a second input terminal connected to the second node, that receives the external clock signal and passes the external clock signal to a third node;

a PMOS transistor having a source terminal connected to a supply voltage, a gate terminal connected to the second node, and a drain terminal connected to the third node;

a delay circuit, having an input coupled to the third node, that delays the
5 passed external clock signal for the predetermined time to provide the delayed external clock signal, and that inverts the delayed external clock signal to provide the inverted delayed external clock signal; and

a NAND circuit that performs the NAND operation on the external clock signal and inverted delayed external clock signal.

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3. The low power flip-flop circuit according to claim 2, wherein the delay circuit is comprised of an odd number of inverters.

4. The low power flip-flop circuit according to claim 2, wherein the
15 PMOS transistor maintains the third node at a high level when the transmission gate is turned off.

5. A flip-flop circuit comprising:

a latch that receives and holds an input signal responsive to an internal
20 clock signal;

a comparison circuit that compares the input signal to an output of said latch and provides a comparison signal indicative thereof; and

an internal clock signal generator including

a transmission gate, having an input coupled to the external clock signal, that is switchably responsive to the comparison signal to selectively provide the external clock signal as a transmission gate output signal at a gate output terminal,

5 an inverter circuit, coupled to the gate output terminal, that delays and inverts the transmission gate output signal to provide an inverter output signal, and

a logical gate that performs a logical operation on the external clock signal and the inverter output signal to provide the internal clock
10 signal.

6. The flip-flop circuit of claim 5, wherein said internal clock signal generator further comprises a switch that selectively couples a supply voltage to the gate output terminal responsive to the comparison signal.

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7. The flip-flop circuit of claim 6, wherein the switch is a PMOS transistor having a gate terminal coupled to the comparison signal, a source terminal coupled to the supply voltage and a drain terminal coupled to the gate output terminal.

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8. The flip-flop circuit of claim 5, wherein the inverter circuit comprises a plurality of inverters connected together in series.

9. The flip-flop circuit of claim 8, wherein the inverter circuit comprises an odd-number of inverters.

10. The flip-flop circuit of claim 5, wherein the logical gate provides the
5 internal clock signal as having pulse width smaller than pulse width of the external clock signal and as having rising and falling edges synchronized with the external clock signal.

11. The flip-flop circuit of claim 5, wherein the logical operation is a
10 NAND logical operation.